WHAT IS CLAIMED IS:

1. A field emitter device on a substrate, comprising:

a first insulating layer on the substrate;

a conducting gate layer having a top surface and at least one side surface, disposed on the first insulating layer;

a field emitter tip disposed on the substrate adjacent the first insulating layer and adjacent to the at least one side surface; and

a second insulating layer disposed at least on at least one side surface located adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

2. The field emitter device of claim 1, wherein the first insulating layer comprise one of silicon dioxide, silicon oxynitride and silicon nitride.

3. The field emitter device of claim 1, wherein the second insulating layer covers the top surface of the conducting gate layer.

4. The field emitter device of claim 1, wherein the field emitter tip comprises one of a refractory metal tip, a nanotube and a nanowire.

5. The field emitter device of claim 1, wherein the field emitter tip comprises a nanowire comprising one of ZnO, refractory metal, refractory metal carbides, and diamond.

6. The field emitter device of claim 4, wherein the field emitter tip comprises a refractory metal tip comprising one of molybdenum, niobium and hafnium.

7. The field emitter device of claim 1, wherein the field emitter tip comprises a carbon nanotube.

8. The field emitter device of claim 1, wherein the substrate comprises a semiconductor.

9. The field emitter device of claim 8, wherein the substrate comprises one of silicon, germanium and gallium arsenide.

10. A field emitter array comprising an array of field emitter devices on a substrate, at least one of the field emitter devices of the array comprising:

a first insulating layer on the substrate;

a conducting gate layer having a top surface and at least one side surface, disposed on the first insulating layer;

a field emitter tip disposed on the substrate adjacent the first insulating layer and adjacent to the at least one side surface; and

a second insulating layer disposed at least on at least one side surface located adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

11. The field emitter array of claim 10, wherein the first insulating layer is one of silicon dioxide, silicon oxynitride and silicon nitride.

12. The field emitter array of claim 10, wherein the second insulating layer covers the top surface of the gate conducting layer.

13. The field emitter array of claim 10, wherein the field emitter tip comprises one of a refractory metal tip, a nanotube and a nanowire.

14. The field emitter array of claim 10, wherein the field emitter tip comprises a refractory metal tip comprising one of molybdenum, niobium and hafnium.

15. The field emitter array of claim 10, wherein the field emitter tip comprises a carbon nanotube.

16. The field emitter array of claim 10, wherein the field emitter tip comprises a nanowire comprising one of ZnO, refractory metal, refractory metal carbides, and diamond.

17. The field emitter array of claim 10, wherein the substrate comprises a semiconductor.

18. The field emitter array of claim 17, wherein the substrate comprises one of silicon, germanium and gallium arsenide.

19. A method of forming a field emitter device on a substrate, the method comprising:

forming a first insulating layer on the substrate;

forming a conducting gate layer having a top surface and at least one side surface on the first insulating layer;

forming a field emitter tip on the substrate adjacent the first insulating layer and the conducting layer; and

forming a second insulating layer on at least one side surface of the conducting gate layer adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

20. The method of claim 19, wherein the forming a first insulating layer comprises:

blanket depositing a first insulating material over the substrate; and

patterning the first insulating material.

21. The method of claim 19, wherein the forming a first insulating layer comprises:

growing a first insulating material on the substrate.

22. The method of claim 19, wherein first insulating material comprises one of silicon oxide, silicon nitride and silicon oxynitride.

23. The method of claim 19, wherein the forming a second insulating layer comprises:

blanket depositing a second insulating material over the conducting gate layer; and

patterning the second insulating material.

24. The method of claim 19, wherein the forming a second insulating layer comprises:

selectively depositing a second insulating material on the conducting gate layer.

25. The method of claim 19, wherein the forming a second insulating layer comprises:

selectively depositing a second insulating material on the gate conducting layer and the first insulating layer.

26. The method of claim 19, wherein the forming a second insulating layer comprises:

depositing a second insulating material on the gate conducting layer using the first insulating layer and the conducting gate layer as a shadow mask.

27. The method of claim 19, wherein the forming a second insulating layer further comprises:

forming the second insulating material over the top surface of the conducting gate layer.

28. The method of claim 19, wherein the second insulating layer comprises silicon oxide, silicon oxynitride or silicon nitride.

29. The method of claim 19, wherein the forming the conducting gate layer comprises:

depositing a conducting material on the first insulating layer; and

patterning the conducting material to form the conducting gate layer.

30. The method of claim 29, wherein conducting material comprises a refractory metal.

31. The method of claim 19, wherein the forming a field emitter tip comprises:

depositing a conducting material on the substrate; and

patterning the conducting material.

32. The method of claim 31, wherein conducting material comprises a refractory metal.

33. The method of claim 19, wherein the forming a field emitter tip comprises:

forming one of a nanotube and a nanowire on the substrate.

34. The method of claim 19, wherein the forming a field emitter tip comprises:

forming the field emitter tip after forming the second insulating layer.

35. The method of claim 19, wherein the forming a second insulating layer comprises:

forming an anodic oxide on the conducting gate layer.

36. The method of claim 19, wherein the forming a second insulating layer comprises:

forming the second insulating layer on the at least one side surface, but not on the top surface.

37. The method of claim 19, wherein the forming a first insulating layer and the conducting gate layer comprises:

forming a first insulating material;

forming a conducting gate material;

patterning the first insulating material and the conducting gate material at the same time.

38. A field emitter device on a substrate, comprising:

a first insulating layer on the substrate;

a conducting gate layer having a top surface and at least one side surface, disposed on the first insulating layer;

a field emitter tip disposed on the substrate adjacent the first insulating layer and adjacent to the at least one side surface; and

an arc prevention layer disposed at least on at least one side surface located adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

39. The field emitter device of claim 38 wherein the arc prevention layer comprises a semiconductor material.

40. A field emitter array comprising an array of field emitter devices on a substrate, at least one of the field emitter devices of the array comprising:

a first insulating layer on the substrate;

a conducting gate layer having a top surface and at least one side surface, disposed on the first insulating layer;

a field emitter tip disposed on the substrate adjacent the first insulating layer and adjacent to the at least one side surface; and

an arc prevention layer disposed at least on at least one side surface located adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

41. The field emitter array of claim 40 wherein the arc prevention layer comprises a semiconductor material.

42. A method of forming a field emitter device on a substrate, the method comprising:

forming a first insulating layer on the substrate;

forming a conducting gate layer having a top surface and at least one side surface on the first insulating layer;

forming a field emitter tip on the substrate adjacent the first insulating layer and the conducting layer; and

forming an arc prevention layer on at least one side surface of the conducting gate layer adjacent the field emitter tip to prevent arcing between the field emitter tip and the conducting gate layer.

43. The method of claim 42 wherein the arc prevention layer comprises a semiconductor material.